ABSTRACT OF THE DISCLOSURE

There is provided a semiconductor memory device capable of performing high-speed reading even when the current capability of memory cells and transistors for charging is decreased, and a bit line capacitance is increased. In a sense amplifier, in addition to a P-type MOS transistor for charging, a P-type MOS transistor and a N-type MOS transistor are provided as a circuit for charging a selected bit line up to a switching level of a determination inverter included in a circuit for determining data of a memory cell, and a bit line is charged at high speed, whereby a read time is shortened.